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The design of the Instrument Control Unit and its role within the Data Processing System of the ESA PLATO Mission

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ABSTRACT

PLATO[1] is an M-class mission of the European Space Agency's Cosmic Vision program, whose launch is foreseen by 2026. PLAnetary Transits and Oscillations of stars aims to characterize exoplanets and exoplanetary systems by detecting planetary transits and conducting asteroseismology of their parent stars.

PLATO is the next generation planetary transit space experiment, as it will fly after CoRoT, Kepler, TESS and CHEOPS; its objective is to characterize exoplanets and their host stars in the solar neighbors. While it is built on the heritage from previous missions, the major breakthrough to be achieved by PLATO will come from its strong focus on bright targets, typically with $m_v \leq 11$. The PLATO targets will also include a large number of very bright and nearby stars, with $m_v \leq 8$. The prime science goals characterizing and distinguishing PLATO from the previous missions are:

- the detection and characterization of exoplanetary systems of all kinds, including both the planets and their host stars, reaching down to small, terrestrial planets in the habitable zone;
- the identification of suitable targets for future, more detailed characterization, including a spectroscopic search for biomarkers in nearby habitable exoplanets (e.g. ARIEL Mission scientific case, E-ELT observations from Ground);

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- a full characterization of the planet host stars, via asteroseismic analysis: this will provide the Community with the masses, radii and ages of the host stars, from which masses, radii and ages of the detected planets will be determined.

These ambitious goals will be achieved by ultra-high precision, long (few years), uninterrupted photometric monitoring, in the visible light, of a very large sample of bright stars, which can only be done from space. The resulting high-quality light curves will be used to detect planetary transits and measure their characteristics, as well as to provide a seismic analysis of the host stars, from which precise measurements of their radii, masses, and ages will be derived. For the brightest targets, planets are also expected to be detectable through the modulation of stellar light reflected on the planet surface, and/or through the astrometric wobble induced on the star by the planet orbital motion and measured thanks to accurate centroiding algorithms. Both these techniques can be exploited thanks to ultra-accurate differential photometric measurements.

The PLATO space-based data will be complemented by ground-based follow-up observations, in particular very precise radial velocity monitoring, which will be used to confirm the planetary nature of the detected events and to measure the planet masses. The full set of parameters of the exoplanetary systems will thus be measured, including the main characteristics of the host stars and their orbits like radii, masses, and planets ages.

Measurements of the radii and masses will be used to derive the planet mean densities and therefore will give insight on their internal structure and composition. The orbital parameters, together with the precise knowledge of all characteristics of the host star, will enable the PLATO Science Team to estimate the temperature and radiation environment affecting the planets. Finally, the knowledge of the age of the exoplanetary systems will allow to put them in an evolutionary perspective and compare the achieved results with those coming from the interplanetary Missions exploring our own Solar System.

Keywords: Exoplanets, Transit Photometry, Instrument Control, Data Processing, SpaceWire network.

1. INTRODUCTION

The main scientific requirement to detect and characterize a large number of terrestrial planets around bright stars plays a key role in defining the PLATO observing strategy and its own Payload. The current baseline observing plan for the 4-years nominal science operations consists of long-duration observations of two sky fields lasting two years each. An alternative scenario is for operations split into a long-duration pointing lasting three years and a one-year step-and-stare phase with several pointings. Long pointings will guarantee the detection of planets down to the habitable zone of solar-like stars with a first basic assessment of the main characteristics of their atmospheres, opening the way to future space missions designed to perform spectroscopy on these targets.

The instrumental concept proposed by the PLATO Payload Consortium is based on a multi-camera approach, involving a set of several "normal" instruments monitoring stars fainter than m_v=8, plus a low number of "fast" instruments observing extremely bright stars with magnitudes brighter than m_v=8. The Payload's telescope concept (collecting 24 normal telescopes plus 2 fast telescopes) is based on fully dioptric designs, working in an extended visible light range. It has been designed to observe a very large field, with respect to a sufficient pupil diameter.

The 24 normal cameras are arranged in four sub-groups of 6 cameras. All 6 cameras of each sub-group have exactly the same Field of View (FoV) of about 38 degrees and the lines of sight of the four sub-groups are tilted by $\pm 9{,}2^\circ$ with respect to the Instrument Line of Sight (LoS). This particular configuration allows surveying a very large field at each pointing, with various parts of the field monitored by 24, 18, 12 or 6 normal telescopes and cameras.

This strategy optimizes both the number of targets observed at a given noise level and their brightness. The satellite will be rotated around the mean line of sight by 90° every 3 months, resulting in a continuous survey of exactly the same region of the sky.

Each camera is equipped with its own CCD focal plane array, comprised of 4 CCDs. The CCDs work in full-frame mode for the normal cameras, and in frame-transfer mode for the fast cameras. Each FPA is associated to a Front End Electronics (FEE).

There are several units, the Ancillary Electronics Units (AEUs), which provide secondary voltages to the FEEs. 2 N-AEU boxes provides voltages for the normal FEEs/cameras, one N-AEU for one batch of 12 normal cameras. One F-AEU provides the voltages for the two fast FEEs/cameras. Additionally the F-AEU contains a synchronization module which provides hardware synchronization signals to the FEEs (synchronizing the CCD read-out), power supplies (synchronizing the DC/DC converters) in the AEU and to the Service Module (synchronizing the thermal control system of the Telescope Optical Units, TOUs).

2. THE PLATO DATA PROCESSING SYSTEM

The PLATO Payload Data Processing System (DPS) is made up of the DPUs (Data Processing Units) and the ICU[2,3] (Instrument Control Unit), with data routed through a redundant SpaceWire (SpW) network. The ICU is connected to the Service Vehicle Module (SVM) through four SpW links. These links are independent from the DPS SpaceWire network as the SVM has no direct connection to the other DPS Units, except the Attitude and Orbit Control System (AOCS) interface to two fast DPUs, gathered in one electronic box named FEU (Fast Electronic Unit).

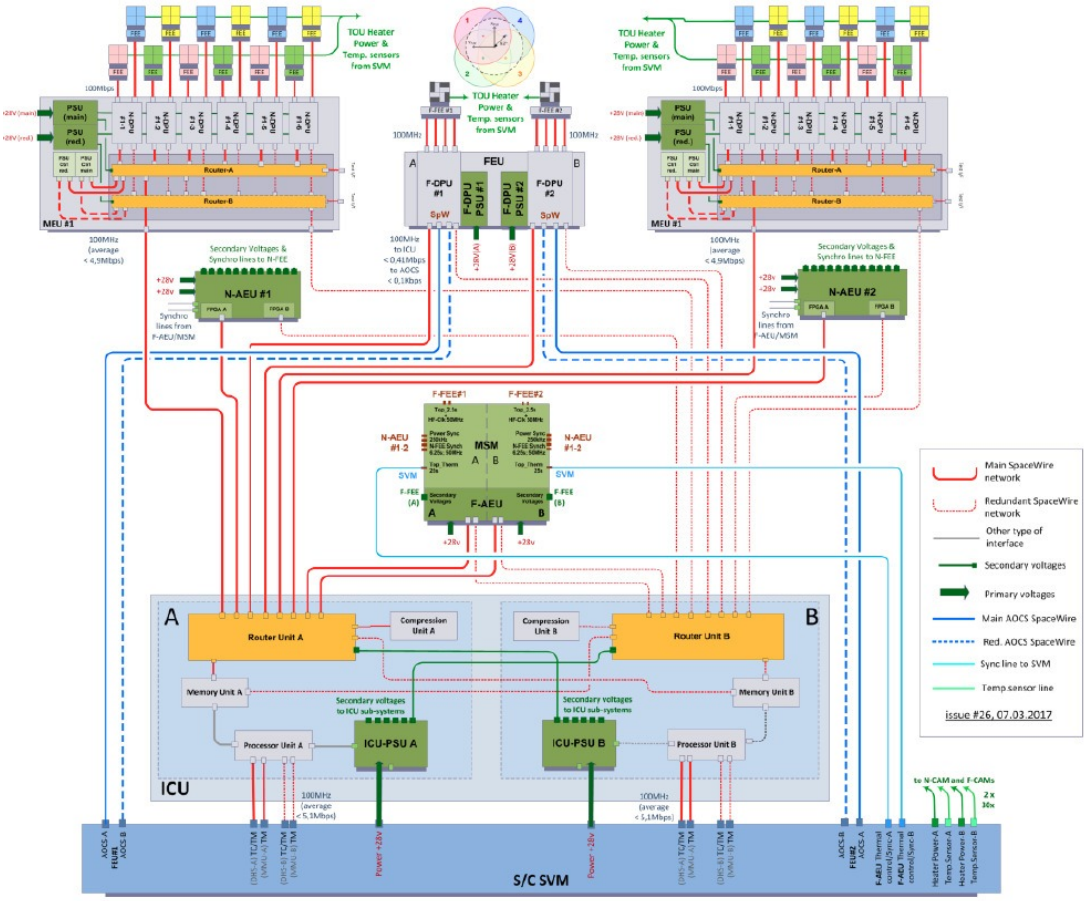

Figure 1. The PLATO Data Processing System architecture, based on a redundant SpaceWire network (links in red color, solid: Nominal, dotted: Redundant).

Each F-DPU is responsible for processing the data of one fast camera. The processing cadence for F-DPUs is 2.5 sec. F-DPUs have a supplementary function: they are responsible for providing angle/attitude error measurements data, as Fine Guidance System (FGS), directly to the SVM AOCS.

The ICU is responsible for the management of the Payload, the communication with the Service Module and the compression of scientific data before transmitting them as telemetry to the SVM. There are 2 ICU channels, gathered in a same box, which work in cold redundancy and 12 normal DPUs. The SpaceWire routers in the two cold redundant ICU chains can be used in a cross-strapped configuration, e.g. ICU A can use the router from ICU B and vice versa.

Each N-DPU is responsible for processing the data of 2 normal cameras and their processing cadence is nominally 25 sec.

After processing, the science data from each N/F-DPU is downloaded to the ICU, which stacks, compresses and then transmits them to the SVM for downloading to Ground. Data from all individual telescopes are transmitted thanks to the S/C on-board transponder to Earth, where final instrumental corrections, such as jitter correction, are performed.

Several photometry algorithms are planned to run on-board, each star being allocated one of them, depending on its brightness and local level of blending.

Fig. 1 presents the PLATO Payload Architecture. It gives an overview of the PLATO Data Processing System with focus on the SpW network. All the units of the Payload are connected each other via SpW links and routers.

Due to fault tolerance reasons and in order to optimize the resources (mass, volume, harness), the physical implementation of the described architecture foresees to split the 12 N-DPUs in 2 groups of 6 N-DPUs. Each group of 6 N-DPUs is gathered in a box called Main Electronic Unit (MEU). Also the SpaceWire routers in the two MEUs are redundant.

2.1 The Instrument Control Unit role

It is worth noting that the ICU plays a key role in managing the data streams and processing tasks across the entire SpW network, which consists of many nodes and data links. The PLATO SpW network architecture turns out to be crucial for several design issues:

- efficient data handling (scientific data, TM and HK);
- harness complexity;
- mass and power limitation.

Due to the number of data links to be handled, the ICU Router Unit implements an 18-channel SpW router. The SpW router is capable of handling the data streams from the CCD detectors to the ICU in an effective and fast way. The SpW network configuration can be set-up via Remote Memory Access Protocol (RMAP) commands from the ICU CPU to the router component and the associated control FPGA.

It is the responsibility of the ICU Application SW (ASW) to configure the whole DPS SpaceWire network including all routers in order to achieve the correct data transfer within the Payload. For that purpose, each DPS Units needs a unique SpW node address. For communication on the SpaceWire network two different protocols are used:

- Remote Memory Access Protocol and
- CCSDS packet transfer protocol.

Both RMAP and CCSDS packets are encapsulated in SpW packets. A CCSDS packet contains an APID and a source or destination identifier. Each DPS unit uses a unique APID for their telecommands (TC) and telemetry (TM) packets. In case of telecommands from the SVM to the PLATO Payload units, the ICU takes the APID to determine the associated SpW node address.

2.2 ICU design

The Instrument Control Unit of PLATO is an integrated box that contains two electronics chains working in cold redundancy. The main functions of the ICU are the following:

- Communicate with the Spacecraft (S/C) via SpW links for telecommands and telemetry;
- Execute telecommands and forward them to the Data Processing System;
- Collect scientific and housekeeping data from PLATO DPS and P/L Units;
- Compress scientific data and send them to the S/C;
- Monitor the status of the payload and provide it as telemetry;
- Perform FDIR (Fault Detection, Isolation and Recovery) tasks and On-board Control Procedures (OBCP) for the overall PLATO payload.

The S/C provides nominal and redundant +28 V supply voltages to the ICU, which generates internal secondary voltages for its sub-modules. The ICU is the interface between the PLATO SVM and the Payload and, considering the high amount of data and the needed data rate, also the communication between the ICU subsystems is based on an internal SpW network. Fig. 2 shows a block diagram of ICU data and power interfaces as well as its system architecture, as designed by Kayser Italia (ICU industrial Prime Contractor).

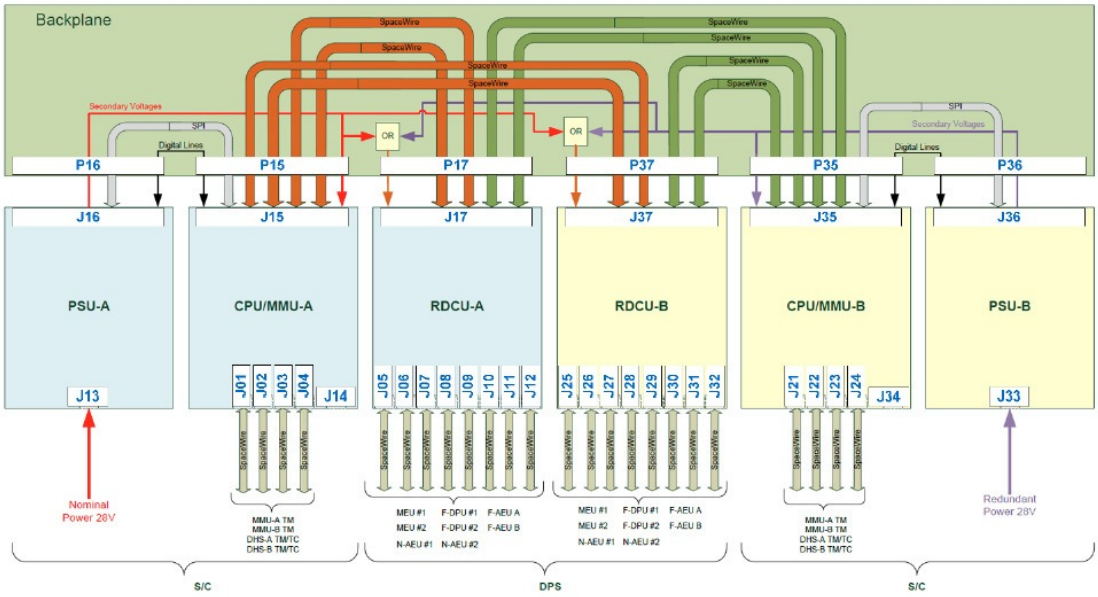

Figure 2. ICU architecture block diagram.

It consists of 3 nominal + 3 redundant modules in a cold redundancy configuration. Modules tagged as A are nominal and modules tagged as B are redundant. Their main functions are the following:

- Nominal Power Supply Unit (PSU-A): it receives the +28 V from the S/C and provides the secondary supply voltages to the A modules;
- Nominal Processor and Mass Memory Unit (CPU/MMU-A): it is the main data processing module of the ICU. It is responsible for Payload control and for interfacing the S/C for telecommands and telemetry;

- Nominal Router and Data Compressor Unit (RDCU-A): it implements a SpW router to put in communication the CPU/MMU module with the rest of PLATO DPS and it performs a data HW compression (FPGA-based) in order to reach the compression requirements of the ICU;
- Single Back-Plane (BP): it allows the power distribution and the data sharing between the described modules.

Cold redundant boards have the same function of the nominal ones.

RDCU-A and RDCU-B are the only ICU modules in cross-strapping configuration for power and data. Each RDCU can be powered by both PSUs (A and B) thanks to the power OR function implemented in the Unit design. Each PSU implements power switches to power on/off the desired RDCU. These switches are under control of the CPU/MMU board by means of discrete digital signals. Each PSU communicates with the related CPU/MMU (CPU/MMUA with PSU-A and CPU/MMU-B with PSU-B) via SPI for housekeeping data transfer (voltages, currents and temperatures), which are eventually provided to the S/C by means of HK telemetry.

Each CPU/MMU communicates with both RDCUs by SpW links:

- two SpW links between CPU/MMU-A and RDCU-A;
- two SpW links between CPU/MMU-A and RDCU-B;
- two SpW links between CPU/MMU-B and RDCU-A;
- two SpW links between CPU/MMU-B and RDCU-B.

Only one communication configuration of two SpW links of the above list can be active at a time, according to which modules are powered.

The overall ICU architecture was defined trying to meet all the PMC specified requirements and it actually represents the result of a trade-off study carried out in terms of computing capability, flexibility, design complexity and reliability in order to comply with the allocated budgets (power consumption, mass and volume).

2.2.1 Mechanical design

The baseline ICU architecture has been designed for its implementation within a single box internally redundant, as shown in Fig. 3. Each electronic chain is composed by three boards, plus a common back-plane for signals routing. All the boards are perpendicularly plugged onto a back-plane fixed by means of screws on the unit back panel. The box dimensions are 293 x 260 x 245 mm^3 (X, Y, Z), without considering the bonding stud.

The electronic boards will be stiffened by a proper mechanical frame (refer to Fig. 4) with the external I/O connectors fixed and screwed to the board upper panels and the lateral sides of the modules will be equipped with card lock retainers, used to fix the boards to the unit mechanical frame and to conduct and dissipate heat towards the Unit baseplate.

The ICU box is composed of four walls and a back panel assembled together through M4 screws. All panels are made of Aluminium alloy AA6061-T651 surface treated with chromatization (Alodine finish as baseline). The back panel hosts the back-plane board, while left and right walls support the card retainers; the thickness of such walls and in particular of the internal ribs is therefore designed to cope with the heat dissipation needs.

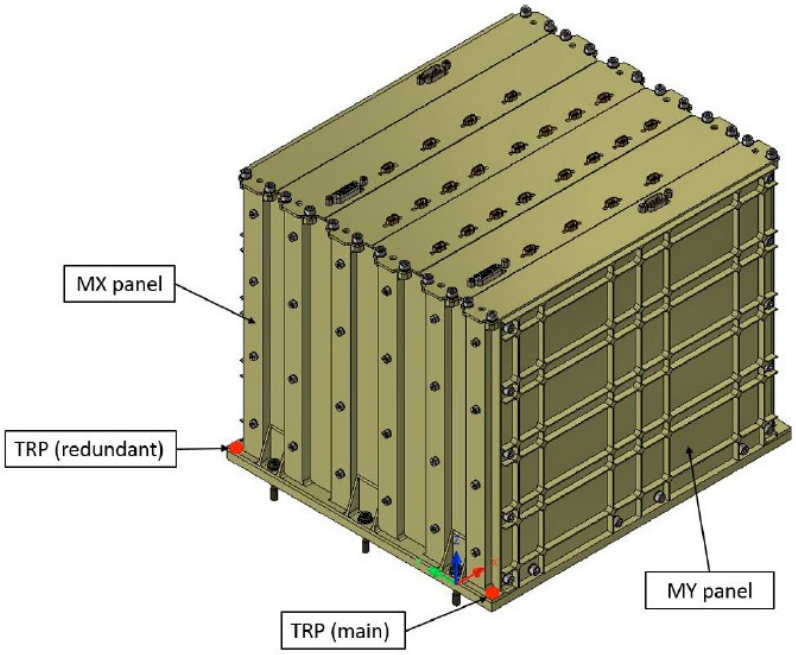

Figure 3. ICU box mechanical design, showing the location of the Temperature Reference Points (TRP) adopted for thermal analysis.

The ICU box is provided with 8 venting holes with 3 mm diameter as they shall be as small as possible (to avoid contaminants to enter) and located as close as possible to the unit mechanical mounting plane interfacing the SVM bench, to which is fixed by two rows of five captive titanium M5 screws.

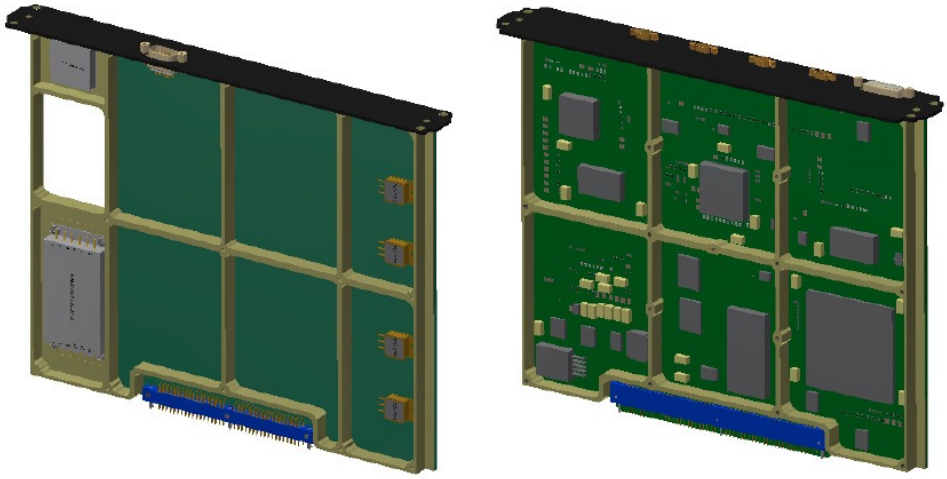

Figure 4. PSU and CPU/MMU boards with their mechanical frames for stiffness improving.

2.2.2 Power Supply Board

The Power supply board (refer to Fig. 5) is based on DC/DC converters and it consists of three sections.

1. Power conditioning section with:
    - Polarity inversion protection;
    - Inrush current limitation;
    - Latching over current protection;
    - EMI filtering;
    - DC/DC conversion with 2 independent DC/DCs: a main DC/DC for the generation of the +5 V to be distributed to the other boards and an Aux DC/DC for powering of internal logic (HK section), acquisition of voltages/currents/temperatures housekeeping, and for power protection circuits.
2. Power distribution section with:
    - Over-voltage protection;
    - 3 built-in Over Current Breakers (OCB) with embedded power switches.
3. HK acquisition section with:
    - Two 12-bits analog to digital converters (ADCs) controlled by the processor via SPI bus for voltage, current and temperature measurements.

Temperature sensors (thermistors) are used for PSU and CPU/MMU boards as well as RDCU. Each PSU can provide power to both SpW Router boards. Which router is going to be powered (N or R) is controlled by the Processor board via discrete commands (CPU GPIO port).

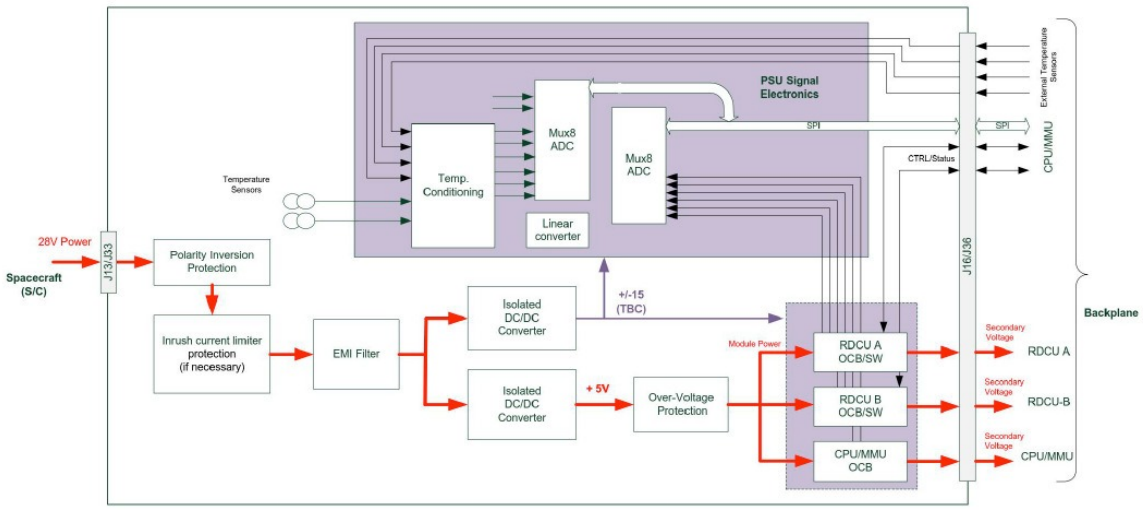

Figure 5. Power supply board design.

CPU/MMU and RDCUs are basically supplied by a main voltage level of +5 V protected for over-voltage and over-current. The secondary voltage levels needed by the hosted electronic components are locally derived by means of Point of Load (PoL) and linear converters.

The ICU is responsible for acquiring its own secondary voltages levels and current consumptions and it will also collect the HK data coming from the other subsystems. All housekeeping data will be transmitted to S/C as telemetry.

It is not foreseen the monitoring of the primary voltage (+28 V) and current levels feeding the ICU PSU as it is assumed that this kind of measurement is directly performed by the SVM.

2.2.3 Processing and Mass Memory Board

The CPU board (refer to Fig. 6) is based on the UT700 (LEON3FT) SPARC V8 microprocessor, produced by Cobham, running at 133 MHz, as required by the processing needs estimates and SVM I/Fs requirements. The processor is indeed provided with 4 embedded SpW links allowing to be directly interfaced to the S/C SVM.

The UT700 is connected to the following memories:

- 128 kB of PROM: it is used to store the Boot Software (BSW);
- 16 MB of MRAM: it is used to store at least two images of the ICU Application Software and external DPUs ASW. It will contain also payload parameters and data (e.g. the star catalog);
- 8 MB of SRAM, as baseline: it is used mainly to run the ASW;
- 512 MB of SDRAM: it is used as buffer by the ASW for data transfer.

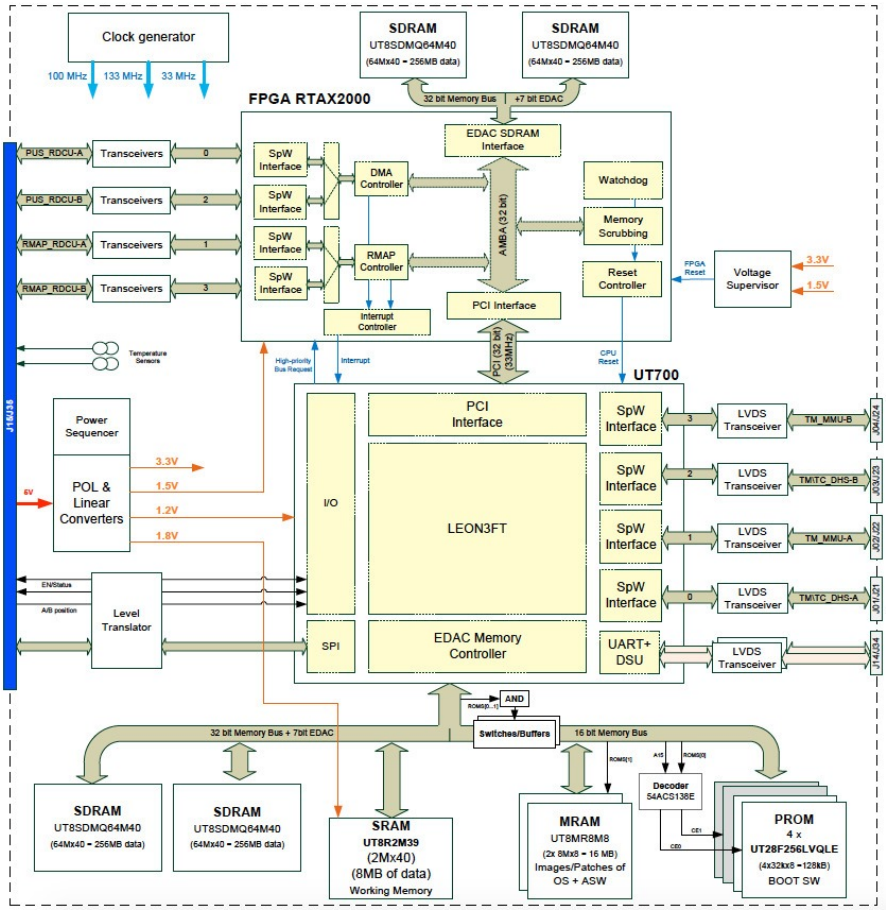

Figure 6. The CPU and MMU board architecture.

SDRAM and RAM memories are EDAC protected by the memory controller of UT700 with a bus of 40 bits wide (32+8 bits for EDAC function).

Due to the selected SDRAM devices and the Processor features, UT700 is able to address only 512 Mbyte of data, so an FPGA is used to interface other 512 Mbyte of SDRAM in order to reach the required total mass memory of 1 GB (Gbyte).

The FPGA expands the processing, communication and storage capabilities of the processor implementing another SDRAM controller and additional SpW links, including DMA controllers, to perform high-speed data transfer from/to RDCU. The FPGA is based on a RTAX2000S and is interfaced with the UT700 by means of a 32 bit wide, 33 MHz, PCI bus.

As above reported, only 2 links of the 4 available SpW interfaces are active at the same time. Two SpWs are connected to RDCU-A and two to RDCU-B. Two links for a single RDCU (nominal or redundant) are requested to separate the data encoded in different protocols: one SpW is dedicated to RMAP protocol and the other one to a Packet Utilization Standard (PUS) protocol.

The FPGA architecture is based on an internal AMBA bus at 32 bit/33 MHz that allows the needed peripherals to be connected together with the processor. All FPGA peripherals have an AMBA interface to standardize the internal communication and data transfer.

The internal FPGA blocks are:

- PCI target interface: it interfaces the UT700 CPU with the internal peripherals of the FPGA. It implements a sort of bridge between the external PCI bus and the internal AMBA bus;
- RMAP controller, interfacing a single SpW link at a time implementing the RMAP initiator;
- Generic DMA controller interfacing a single SpW link at a time for data transfer in PUS format;
- Memory Scrubber: scrubbing engine performing autonomous scan of a programmable region (by addressing) of the memory, reading and writing back the data in order to avoid error accumulation;
- EDAC SDRAM controller: it is used to address the SDRAM connected directly to the FPGA;
- Interrupt controller: it provides an interrupt to the processor in order to schedule and optimize low-level software procedures involving the FPGA peripherals. It provides also some configuration registers accessible, from the CPU, by means of the AMBA/PCI bus;
- Watchdog and Reset controller: in combination with a dedicated voltage supervisor chip it provides the reset to the processor at power-on and during nominal operations in case of software dead-lock.

2.2.4 Routing and Data Compression Board

The RDCU is part of the ICU and, besides managing the DPS SpW network, provides an FPGA-based hardware compressor for the cropped imagettes around the target stars and full CCD images acquired by the PLATO cameras. Each ICU Router Unit (RDCU-A and RDCU-B) is connected to the DPS and P/L sub-units throughout eight SpW links, used to interface:

- 2 F-AEUs
- 2 FEUs/F-DPUs
- 2 MEUs where RDCU-A is connected to MEU routers A and RDCU-B to MEU routers B (each MEU contains two routers)
- 2 N-AEUs

The main components of an RCDU board are:

- a SpW router for managing the data flow between the ICU and the DPS sub-units;
- an FPGA for data compression, SpW link control and providing HK information;
- an on-board memory (SRAM-type) for storing compression data and models;

- PoL converters for generating the required board voltages from the supply voltage;
- an ADC for gathering HK data.

The RDCU board is supplied with a nominal voltage of +5.0 V generated by the PSU. All other voltages (+3.3 V for the digital components; supply voltages for SpW Router, SRAM and FPGA) are generated directly on the RDCU board by means of point of load converters.

Fig. 7 shows a functional block diagram of the RDCU components. The selection of the active RDCU is controlled thanks to the CPU board, which is in charge of switching on and off the HW compression cores.

The router section is implemented by means of the new ASIC device, the GR718B, from Cobham hosting 16x SpW ports with on-chip LVDS plus 2x LVTTL ports. It is characterized by a non-blocking switching matrix connecting any input port to any output port for packets and system time distribution as well. Each port has a timer to recover in case of deadlock.

The router is connected to the CPU/MMU board by means of 2 SpW links allowing the RMAP protocol access to all the DPS subsystems, N/F-AEU. Indeed, a cross strapping with CPU/MMU Units (N and R), involving 2 + 2 SpW links, is foreseen (refer to Fig. 6), as described in the previous paragraph.

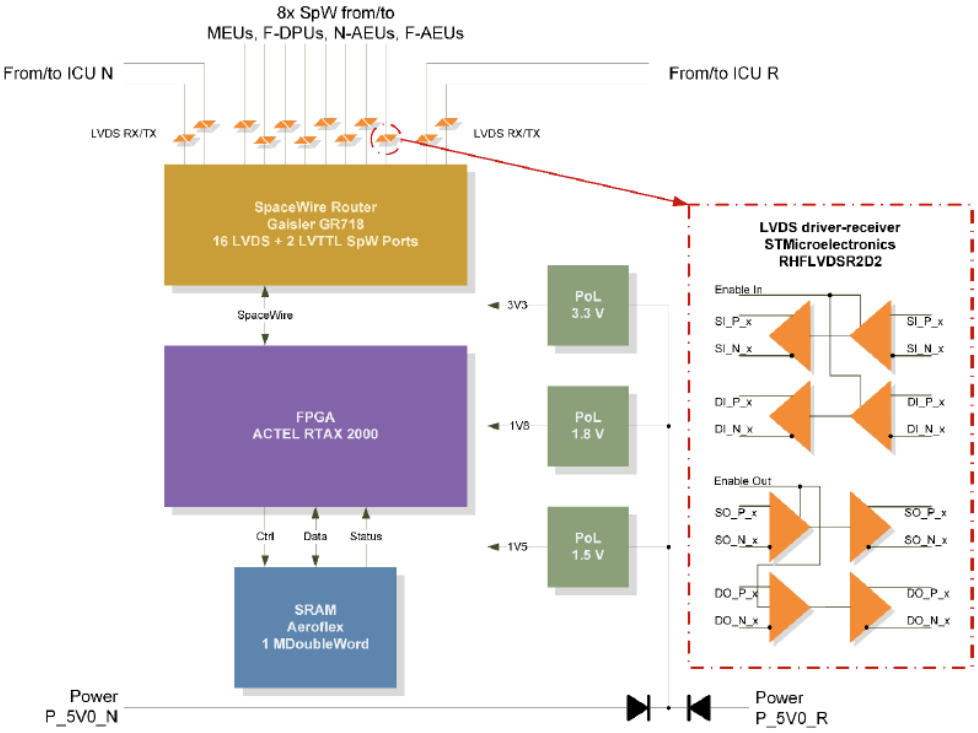

Figure 7. RDCU board block diagram with focus on SpW transceivers.

The SpW Router board is interfaced to the CPU by means of a sort of cPCI-SpW bridging logic (supporting RMAP; the compression task is started by accessing to the FPGA control register via RMAP) operating inside the CPU/MMU board FPGA. The latter implement 2N + 2R SpW interfaces (FPGA based, actually 2 SpW IP cores) supporting RMAP (1N and 1R): the processor can generate RMAP commands towards the Router board and towards the overall DPS or access the local resources by means of the RMAP protocol.

Each PSU can provide power to both Router boards. Which router is going to be powered is controlled by the CPU board via discrete commands on the GPIO port (it can be operated a selection by the S/C OBC through dedicated TCs).

2.2.5 Back plane

The back-plane hosts the connectors for all the ICU boards, acting as a routing board for power, digital and analog signals. It represents the mean through which the Nominal and Redundant boards are connected and share the power and signal lines.

Thanks to the use of the back-plane, all the I/O connectors are directly mounted on the relevant PCB modules and there are no wired connections inside the unit. The back-plane is equipped with straight connectors with a pin assignment in order to limit crosstalk noise and spurious signals between power and signal lines and it lies on the unit bottom panel, while the modules are inserted through the top of the ICU box and plugged onto the same back-plane.

2.3 Conclusion

In this paper we have shown the PLATO ICU architecture along with its role in the Payload Data Processing System, at the present status of maturity of the Project. The PLATO P/L will undergo the Instrument PDR (Preliminary Design Review) at the end of 2018 and the following Units PDR during the next spring.

Some DPS requirements affecting the ICU design are still open but they will be finely defined and frozen during the present co-engineering Phase, exploiting a collaborative effort involving ESA, PMC and the selected S/C Prime, OHB Bremen.

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